



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED  
JUN 13 2001  
TC 2800 MAIL ROOM

Applicant: Wendell P. Noble et al.

Title: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

Docket No.: 303.379US2

Serial No.: 09/551,027

Filed: April 17, 2000

Due Date: N/A

Examiner: Michael Trinh

Group Art Unit: 2822

Commissioner for Patents  
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ A Supplemental Information Disclosure Statement (1 pgs.), Form 1449 (1 pgs.), and copies of 1 cited references.
- ☒ A check in the amount of \$180.00 to cover the fee for consideration of Information Disclosure Statement under 97(c).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

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By: Edward J. Brooks, III  
Atty: Edward J. Brooks, III  
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 5<sup>th</sup> day of June, 2001.

Name

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